A STRIPLINE KICKER FOR THE NEXT GENERATION LIGHT SOURCE*

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Diversified Technologies, Inc. (DTI) recently completed an SBIR effort under a grant from the US Department of Energy to research kicker drivers for the Next Generation Light Source (NGLS) injectors. The NGLS specification required a 10 kV, 200 Ampere pulse into 50 Ω, with a 2 ns rise time (10-90%), a highly repeatable flattop with a pulsewidth from 5-40 ns, and a fall time less than 1 μs (defined as down to 10^{-4} of the peak value). DTI chose a novel derivative of the classic inductive adder circuit which has demonstrated not only the required pulse rise times required by NGLS, but also the pulses required by the Advanced Light Source (ALS) upgrade at Lawrence Berkeley National Lab (LBNL), and a number of other commercial, medical, and other non-accelerator-based applications.

Keywords : NGLS, Inductive Adder, Stripline Kicker

1. INTRODUCTION

DTI has designed, built, and demonstrated a prototype pulse amplifier for stripline kicker service capable of less than 5 ns rise and fall times, 5 to 90 ns pulse lengths, peak power greater than 13.7 MW at pulse repetition rates exceeding 100 kHz, and measured jitter under 100 ps. The resulting pulse is precise and repeatable, and will be of great interest to accelerator facilities requiring electromagnetic kickers. The unit has also seen interest from manufacturers of medical devices, particularly those interested in the generation of short-lived plasmas.

The pulse generator is based on the original specifications for the NGLS fast deflector. DTI's planar inductive adder configuration uses state of the art compensated-silicon power transistors in low inductance leadless packages with a novel charge-pump gate drive to achieve unmatched performance. Full-scale modelling and prototyping efforts revealed a number of issues impossible to detect in initial, simplified, single-stage efforts. The prototyping efforts in the first years of the program guided the design of the full unit, however the magnetics and transmission line effects of the system were not revealed until the entire unit was assembled. The unit was brought to LBNL, compared with other researcher's efforts at LBNL, and was judged very favorably. A number of development prototypes have been constructed and tested, including the successful 18.7 kV, 749 A unit described in this paper.

DTI's final design, a single board stuffed with the appropriate transistors and operated under the correct conditions, met many of the original design goals, though admittedly not necessarily all at the same time. The fastest rise time measured at 10 kV with this topology to date exceeds 4 ns 10-90%, however, this is limited primarily by the clamp diodes rather than intrinsic device physics (which will be discussed in detail later in this paper). The peak repetition rate is over 100 kHz, and the burst rate is limited only by core reset in the inductive adder, with a pulse spacing minimum of 3 μs. Due to the intrinsically floating output of the inductive adder topology, the pulse output can operate as positive, negative, or bipolar depending on the application and customer requirement.

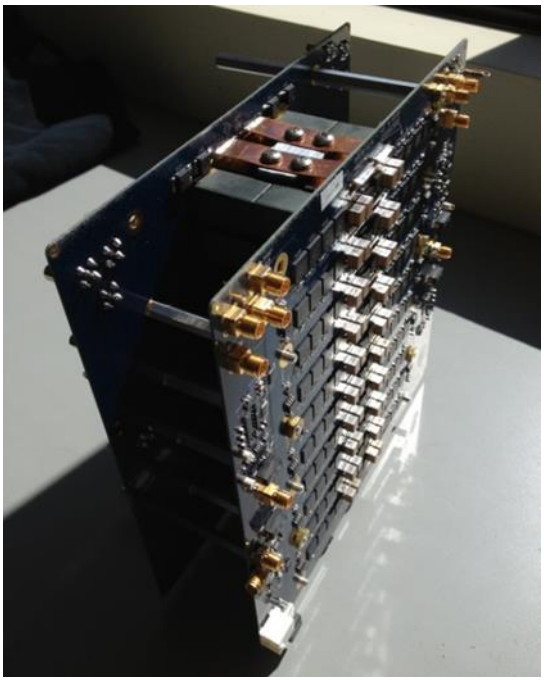

Fig. 1. Dual PCB high speed pulser kicker driver system developed by DTI for the NGLS program. This kicker uses commodity 650 V transistors to switch nearly 17 MW, 700 A in 5 ns.

This high performance, flexible, reliable, and easily manufactured high speed kicker enables DTI to develop high speed pulsers which are readily applicable to present and future collider systems. The modularity of DTI's design also enables configuration of systems for a wide range of potential applications beyond accelerators which require high speed pulsing, including high performance radars, directed energy systems, and excimer lasers.

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2. DESIGN

Inductive adders have been used for decades in the accelerator physics community to create ultra-high voltage, short rise time deflection pulses in beams. The inductive adder approach can be thought of as a number of pulse transformers with the primary windings in parallel and the secondary windings in series. Such approaches are not typically used in high-PRF applications, and have not shown the fast rise times required for the NGLS kicker. DTI's improvements to the classic inductive adder design include:

- Multiple cores on a single circuit board
- Secondary return current path on the circuit board
- State-of-the-art 650 V rated compensated MOSFETs
- Low inductance leadless flat packages
- Push-pull double voltage drive
- Low inductance backswing clamp
- High performance low delay charge pump gate drives

Re-arranging the circuitry of the classic inductive adder by placing several cores and drive circuits on a single circuit board allows the secondary return current to flow through the ground plane on the circuit board, which minizes the secondary stray inductance.

The best figure of merit power transistors are 650 V rated compensated silicon MOSFETs. These are available in very low inductance leadless flat packs. The relatively low voltage rating is compensated for by driving one end of the primary low and the other end high, allowing up to 1 kV added per stage.

At turn-off, the transistor voltage must be limited by a diode backswing clamp. Stray inductance in this circuit allows the voltage to overshoot. This effect can limit the maximum operating voltage, especially with very fast switching times.

The switchng performance of transistors can be limited by the gate drive; DTI developed a low delay, high performance, discrete component gate drive which achieves switching performance much faster than the data sheet values.

Figure 2 shows a simplified schematic of the push-pull circuit. In DTI's final design, four parallel connected MOSFETs drive each side of a primary winding on each stage of the adder. Each individual MOSFET has a diode clamp for overvoltage. All the MOSFETs on each side of each primary share a common high speed gate driver. Isolation for the high side gate drivers is provided using inductive isolation.

3. GATE DRIVER TOPOLOGY

The key innovation is the use of commodity compensated silicon MOSFETs with the state-of-the-art figure of merit (on resistance times gate carge) in low-inductance packages at speeds far beyond the data sheet turn-on and turn-off times. This speed was attained with a custom discrete component gate driver developed at DTI.

Typical commercial MOSFETS have an internal distributed gate resistance of a few ohms. The STL57N65M5, for example, has a gate resistance of 1.4 Ω and gate capacitance of 4.2 nF; the RC time constant is nearly 6 ns. Package and stray circuit inductance also increase the gate charging time. To mitigate these problems, a charge pump circuit is used: a 50 V high current, low delay pulse amplifier drives the gate through a series capacitor sized to deliver the correct gate charge. The effective gate circuit RC time constant is reduced by a factor of 5, allowing switching times much faster than the datasheet values.

The input logic signal is buffered and distributed to the twewnty gate drives on a board through a chain of four 74LVC logic gates, with a total delay of about 6 ns. The gate drive circuit and measured output waveform is shown in Fig. 3. The input transistor of the gate driver, the 20 V rated DMG1012T[i], is driven from both sections of a SN74LVC2G34 buffer. This transistor switches 15 V at 6 A with a propagation delay of less than 2 ns.

The 15 V output from the DMG1012 drives a two transistor totem pole output circuit with IRLML0060 transistors. The first stage drives the bottom transistor directly and top transistor through an inverting transformer. The input transistor is normally off, keeping the bottom totem pole transistor on and the power transistors off.

The pulse transformer is a miniature RF balun with response in the GHz range. This circuit switches 50 V at 35 A with 750 ps rise, 500 ps fall. We also tested a circuit with GaN transistors from EPC.

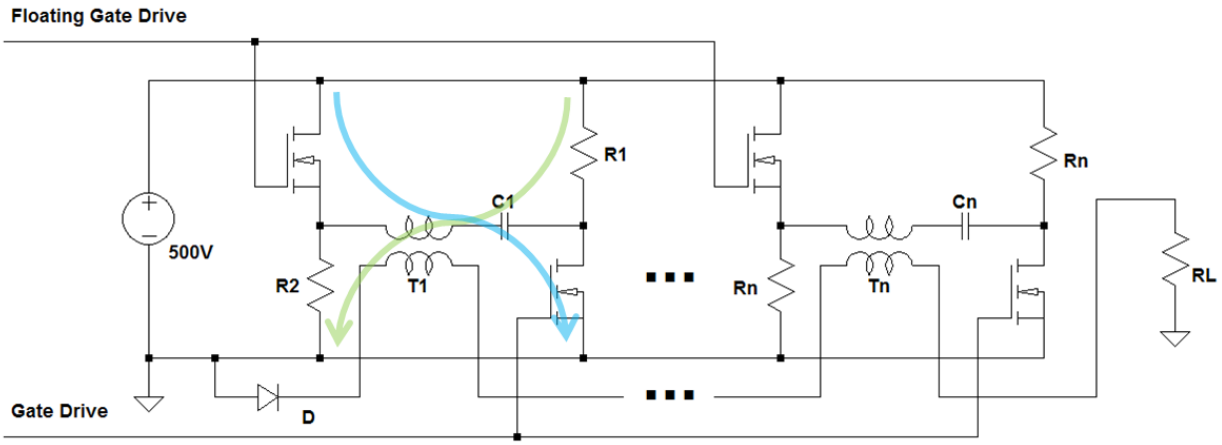

Fig. 2. Electrical schematic of two stages showing main pulse current path in blue and charging current path in green. The floating gate drive is referenced to the source leads of the "flying" transistors. For clarity, snubbers and clamp diodes are not shown. Diode D isolates the transformer core reset voltage from the load.

We selected the silicon circuit for ease of manufacturing with acceptable performance.

4. TRANSISTOR PERFORMANCE

The final layout of the kicker PCBs is shown in Fig. 5. The charge pump gate drive used to push the compensated silicon transistors is quite effective. We tested several types of transistors in the circuit: STL57N65M5, STL21N65M6, and IPL65R130C7 were all demonstrated to have excellent rise and fall times. Faster transistors were less rugged than slower ones due to limitations in the backswing clamp circuit.

The backswing clamp diodes and capacitors are mounted directly undneath the power transistors with multiple vias between layers. SiC diodes in the D2-PAK were used. The board and the transistor only accounted for 1 nH of stray inductance, but the diode package measured 2.4 nH. Thus with all losses accounted, at 40 A, the turn-off spike could only clamp at 154 V even with a

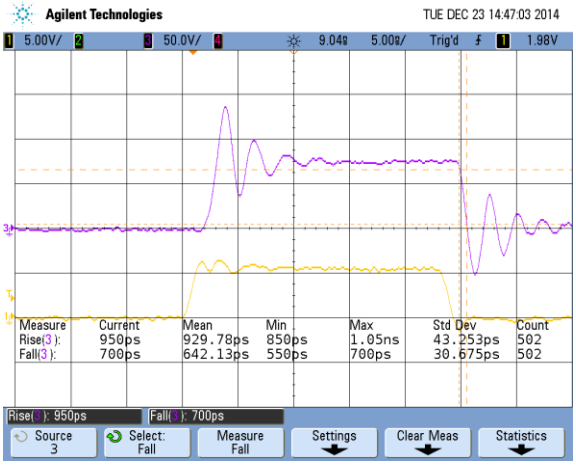

Fig. 3. Peformance of the gate driver circuit with GaN transistors in a test board, operating from 75 V into 1.5 Ω and 3.3 nF, or 50 A peak. Note the 950 ps rise time, 700 ps fall time, and 1.5 ns group delay.

SiC diode directly across the drain of each MOSFET. This ultimately limited our 650 V MOSFETs to safe operation at a maximum of 450 V. A lower inductance diode is required in future development work.

5. CONCLUSION

Given the successes of the pulser demonstrations in the last several months both at LBNL and for various potential commercial customers at DTI, it is DTI's plan to continue development of this core technology. The topology for the pulser coupled with the novel ultra-high-performance gate driver has pushed the inductive adder state-of-the-art. The device physics principles revealed from high speed turn-off in compensated-silicon MOSFETs as it relates to charge storage and clamping capacity of SiC diodes and the theories built around the results from prototype demonstration have been extremely enlightening. Testing of the hardware has pushed the limits of the state-of-the-art in both PCB manufacturing, circuit design, and SPICE simulations. Scaling assumptions made in the initial phases turned out to be prescient in some areas, while completely off-base in others. Prototype after prototype development efforts

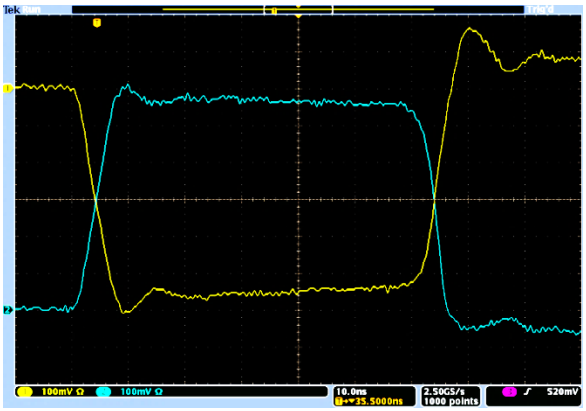

Fig. 4. Bipolar operation of two kicker boards into 50 Ω each side, 5.8 kV (+) and (-), 5 ns rise, 6 ns fall, 30 ns flattop. Due to the simple transformer arrangement of the output, setting up the pulser for bipolar or unipolar operation as simple as moving bolts.

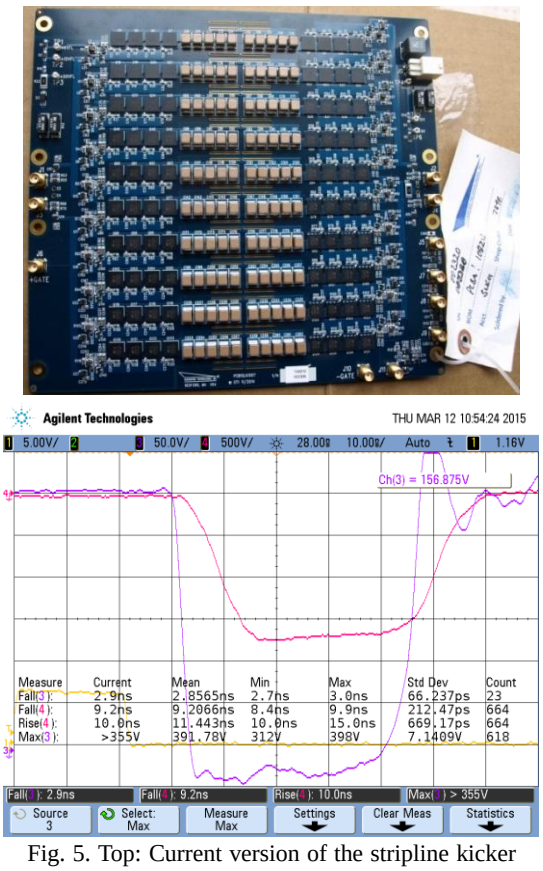

Fig. 5. Top: Current version of the stripline kicker circuit board. Bottom: Representative switching performance of STL57N65M5 transistors at 100 A per transistor. Purple trace (channel 3) shows the drain voltage. Note that the turn on occurs in 2.9 ns. The output pulse is 18.6 kV, 370 A into 50 Ω, or 7 MW per pulse. The pulser was configured with two boards in series for this demonstration, and as such only achieved 9 ns rise and 10 ns fall. With a single board, the system is more than twice as fast; it is limited by the inductance of the secondary.

eventually yielded a pulser that supports full voltage and current at the required PRF and rise and fall times.

Parallel and series operation of two boards and more was successfully demonstrated, and the flexible voltage and repetition rate capability was achieved. Understanding the limitations of our current circuit, we now know how to improve beyond the 6-7 kV limit per board, and the path to sub-5 ns rise and fall times with the full 10 kV per board.

References

i http://www.diodes.com/datasheets/ds31783.pdf Diodes Inc., DMG1012T N-Channel Enhancement Mode MOSFET